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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,498	10/27/2000	Ahmadreza Rofougaran	40886/CAG/B600	3857

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EXAMINER
MILORD, MARCEAU

ART UNIT	PAPER NUMBER
2682	9

DATE MAILED: 08/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,498	ROFOUGARAN ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sutardja et al (US Patent No 5686867) in view of Schlang et al (US Patent No 5890051) and Nardi (US Patent No 5341110).

Regarding claims 1-7, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardia et al does not specifically disclose the feature of a mixer to mix the oscillator output with a second signal to produce a mixed signal; and a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

On the other hand, Schlang, from the same field of endeavor, discloses a mobile phone receiver comprising a first down converter using a first local oscillator frequency which can be tuned in frequency steps by a programmable digital frequency synthesizer PLL that is locked to a reference frequency (col. 3, lines 23-62; col. 7, lines 35-65). The first down converter converts received signals to a first IF for filtering. In addition, Schlang also shows in figure 5, a transmit mixer 46 that mixes the transmit frequency and the first local oscillator frequency to produce a difference frequency signal at the transmit offset frequency (col. 9, line 29- col. 10, line 39; col. 3, line 63- col. 4, line 11; col. 8, lines 15-26; col. 8, lines 27-49; col. 10, lines 29-51)

Nardi also discloses a phase-locking oscillator circuit having improved phase noise characteristics. The oscillator circuit includes a tuned oscillator for providing a carrier signal at a tunable carrier frequency (col. 2, lines 43- 62). Furthermore, Nardi shows in figure 3, a phase detector 116, which operates to generate an error signal based on either the frequency or phase difference between the RF output signal and a reference signal provided by a reference oscillator 124. The error signal is supplied to a loop filter circuit 130 connected in a feedback loop configuration between the YIG tuned oscillator, phase modulator and phase comparator (col. 3, lines 28- 65; col. 4, lines 27- 43; col. 5, lines 2- 22; col. 5, lines 41- 58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Nardi to the modified system of Schlang and Sutardja in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits.

Regarding claims 8-14, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: a tunable oscillator having a tuning input (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardja et al does not specifically disclose the feature of a mixer coupled the oscillator; and a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

On the other hand, Schlang, from the same field of endeavor, discloses a mobile phone receiver comprising a first down converter using a first local oscillator frequency which can be tuned in frequency steps by a programmable digital frequency synthesizer PLL which is locked to a reference frequency (col. 3, lines 23-62; col. 7, lines 35-65). The first down converter converts received signals to a first IF for filtering. In addition, Schlang also shows in figure 5, a transmit mixer 46 that mixes the transmit frequency and the first local oscillator frequency to produce a difference frequency signal at the transmit offset frequency (col. 9, line 29- col. 10, line 39; col. 3, line 63- col. 4, line 11; col. 8, lines 15-26; col. 8, lines 27-49; col. 10, lines 29-51) Nardi also discloses a phase-locking oscillator circuit having improved phase noise characteristics. The oscillator circuit includes a tuned oscillator for providing a carrier signal at a tunable carrier frequency (col. 2, lines 43- 62). Furthermore, Nardi shows in figure 3, a phase detector 116, which operates to generate an error signal based on either the frequency or phase difference between the RF output signal and a reference signal provided by a reference oscillator 124. The error signal is supplied to a loop filter circuit 130 connected in a feedback loop configuration between the YIG tuned oscillator, phase modulator and phase comparator (col. 3, lines 28- 65; col. 4, lines 27- 43; col. 5, lines 2- 22; col. 5, lines 41- 58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Nardi to the modified system of Schlang and Sutardja in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits.

Regarding claims 15-21, Sutardja et al discloses a complimentary metal oxide semiconductor phase lock loop (fig. 1, figs. 10-11, see abstract; col. 2, lines 33- 45), comprising: oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal (col. 3, lines 37- 67; col. 4, line 53- col. 5, line 30).

However, Sutardia et al does not specifically disclose the feature of a mixer means for mixing the first signal with a second signal to produce a mixed signal; and detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

On the other hand, Schlang, from the same field of endeavor, discloses a mobile phone receiver comprising a first down converter using a first local oscillator frequency which can be tuned in frequency steps by a programmable digital frequency synthesizer PLL which is locked to a reference frequency (col. 3, lines 23-62; col. 7, lines 35-65). The first down converter converts received signals to a first IF for filtering. In addition, Schlang also shows in figure 5, a transmit mixer 46 that mixes the transmit frequency and the first local oscillator frequency to produce a difference frequency signal at the transmit offset frequency (col. 9, line 29- col. 10, line 39; col. 3, line 63- col. 4, line 11; col. 8, lines 15-26; col. 8, lines 27-49; col. 10, lines 29-51) Nardi also discloses a phase-locking oscillator circuit having improved phase noise characteristics. The oscillator circuit includes a tuned oscillator for providing a carrier signal at a tunable carrier frequency (col. 2, lines 43- 62). Furthermore, Nardi shows in figure 3, a phase detector 116, which operates to generate an error signal based on either the frequency or phase

difference between the RF output signal and a reference signal provided by a reference oscillator 124. The error signal is supplied to a loop filter circuit 130 connected in a feedback loop configuration between the YIG tuned oscillator, phase modulator and phase comparator (col. 3, lines 28- 65; col. 4, lines 27- 43; col. 5, lines 2- 22; col. 5, lines 41- 58). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Nardi to the modified system of Schlang and Sutardja in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rasmussen US Patent No 5061907 discloses a high frequency CMOS voltage controlled oscillator circuit with gain constant and duty cycle compensation.

Wilcox US Patent No 4642489 discloses a sampled data phase detector using a differential amplifier that is provided with a feedback capacitor connected between the output and the inverting input.

Park et al US Patent No 5937335 discloses a transmission and reception method and apparatus which is capable of supplying local oscillation frequencies for up conversion and down conversion, as well as carrier frequencies for modulation and demodulation by utilizing only one local oscillator.

Ogoro US Patent No 5706315 discloses an automatic frequency control device for tuning the frequency of an intermediate frequency signal to a desired or target frequency.

Nousiainen et al US Patent No 5754560 discloses reliable loop equipment for establishing a test loop for monitoring the condition of a radio station including at least two antennas.

Hrncirik US Patent No 5303394 discloses a Q multiplier circuit, which is automatically feedback, stabilized through the use of phase and gain control loops and adapted for use as an amplifier and filter.

Richmond et al US Patent No 4489413 discloses an apparatus for maintaining a transmit radio signal frequency in a predetermined frequency relationship with a received radio signal.

Ewanus et al US Patent No 3838350 discloses a differential encoded quadriphase demodulator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-305-9508 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

MARCEAU MILORD

Marceau Milord
Examiner
Art Unit 2682

July 27, 2003